High speed and area optimized BISDSR architecture for improved throughput testing applications

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Abstract

The main aim of this project is to effectively represent the difference between two successive frames in video. In order to do so the pixel values of the frames need to be applied to the input of BISDSR (Built in Self Detection and Self Recovery) architecture.This architecture uses bit-split-level implementation code.The video compression technique applied for this design is Motion Estimation and compensation. Using BISDSR gate count can be reduced and speed is improved.

Keywords:*MotionEstimation&compensation,BISDSR architecture,bit-split-levelimplementation,gate count,speed.*

1. Introduction

1.1.Video coding formats:

JPEG, Motion JPEG and MPEG are three well-used acronyms used to describe different types of imagecompression format.A series of techniques – called picture and video

compression techniques – have been derived to reduce this high bit-rate. Their ability to perform this task is quantified by the compression ratio. The higher the compression ratio is, the smaller is thebandwidth consumption. However, there is a price to pay for this compression: increasing compression causes an increasing degradation of the image.

1.2.Two basic standards: JPEG and MPEG

The two basic compression standards are JPEG and MPEG. In broad terms, JPEG is associated with still digital pictures, whilst MPEG is dedicated to digital video sequences. But the traditional JPEG (and JPEG 2000) image formats also come in flavors that are appropriate for digital video: Motion JPEGand Motion JPEG 2000.

The group of MPEG standards that include the MPEG 1, MPEG-2, MPEG-4 and H.264 formats have some similarities, as well as some notable differences.

One thing they all have in common is that they are International Standards set by the ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission.

In the late 1980s the Motion Picture Experts Group (MPEG) was formed with the purpose of deriving a standard for the coding of moving pictures and audio. It has since produced the standards for MPEG 1,MPEG-2, and MPEG-4 as well as standards not concerned with the actual coding of multimedia, such as MPEG-7 and MPEG-21.

1.3.The next step: H.264

At the end of the 1990s a new group was formed, the Joint Video Team (JVT), which consisted of bothVCEG and MPEG. The purpose was to define a standard for the next generation of video coding. When this work was completed in May 2003, the result was simultaneously launched as a recommendation byITU (“ITU-T Recommendation H.264 Advanced video coding for generic audiovisual services”).

MPEG-4 actually consists of many parts, the current one being MPEG-4 part 2. The new standard developed by JVT was added to MPEG-4 as a somewhat separate part, part 10, called “Advanced Video Coding”. This is also where the commonly used abbreviation AVC stems from.

1.4.The basics of compression:

Compression basically means reducing image data.A digitized analog videosequence can comprise of up to 165 Mbps of data. To reduce the media overheads for distributing these

sequences, the following techniques are commonly employed to achieve desirable reductions in image data:

> Reduce color nuances within the image

> Reduce the color resolution with respect to the prevailing light intensity

> Remove small, invisible parts, of the picture

> Compare adjacent images and remove details that are unchnaged between two images

The first three are image based compression techniques, where only one frame is evaluated and compressed at a time. The last one is or video compression technique where different adjacent frames are compared as a way to further reduced the image data. All of these techniques are based on an accurate understanding of how the human brain and eyes work together to form a complex visual system.

As a result of these subtle reductions, a significant reduction in the resultant file size for the image

sequences is achievable with little or no adverse effect in their visual quality. The extent, to which these image modifications are humanly visible, is typically dependent upon the degree to which the chosen compression technique is used. Often 50% to 90% compression can be achieved with no visible difference, and in some scenarios even beyond 95%.

1.5.Frame types:

The basic principle for video compression is the image-to-image prediction.The first image is called an I-frame and is self-contained, having no dependency outside of that image. The following frames may use part of the first image as a reference. An image that is predicted from one reference image is called a P-frame and an image that is bidirectionally predicted from two reference images is called a B-frame.

> I-frames: Intra predicted, self-contained
> P-frames: Predicted from last I or P reference frame
> B-frames: Bidirectional; predicted from two references one in the past and one in the future,and thus out of order decoding is needed.

1.6.Video compression Techniques:

a)Discrete cosine Transform
b)Iterative Logic Array
c)Finite impulse Response filter
d)Motion Estimation and Compensation

a)Discrete cosine Transform:

The first step in image compression, is to divide the image into small blocks, usually of size 8x8 pixels. Then, Discrete Cosine Transform(DCT) is applied on each block to convert each pixel value into frequency domain. It takes 64 input values and yields 64 frequency domain coefficients. This transform is fully reversible; the original block can be reconstructed by applying an InverseDCT(IDCT).

DCT and IDCT are computationally intensive operations, and can take about 30% of processor cycles. But, their memory requirement is very small as they operate on small blocks. Hence, it is ideal to implement them in dedicated hardware co-processors.

Quantization

Quantization is used to discard perceptibly insignificant information. It basically converts each real DCT coefficient to an integer by scaling it by a factor and then discarding the digits after the decimal point. For each coefficient, a scaling factor is chosen in such a way that there is no perceptible change even after discarding digits after the decimal point.

Coding

The next step in the compression process is to encode the DCT coefficients using as few bits as possible. After quantization, most of the DCT coefficients are zeros. This is true for most high frequency DCT coefficients. To take advantage of this, consecutive zeros are grouped and the number of zeros in the group is encoded. This process is called “Run-Length encoding”. To fascilitate run-length encoding, the DCT coefficients are encoded in a zig-zag fashion, starting from top-left and ending at bottom-right.

b)Iterative Logic Array:

An iterative Logic array can be in a single dimension (1D) or multiple dimensions (wavefront and systolic array).Arithmetic functions operate on binary vectors, use the same subfunction in each bit position This Array can design functional block for subfunction and repeat to obtain functional block for overall function.Iterative array works on array of interconnected cells.

c)Finite Impulse Response Filter:

Amongst all the obvious advantages that digital filters offer, the FIR filter can guarantee linear phase characteristics neither analog or IIR filters can achieve this.

- **Filter coefficients:**

$$y[n]=\sum_{k=0}^{N-1} b_k \cdot x[n-k]$$

x[n] represents the filter input,
bk represents the filter coefficients,
y[n] represents the filter output,
N is the number of filter coefficients (order of the filter).

d)Motion Estimation and compensation:

In videos like news programs, there is very little change from frame to another. Video codecs can take advantage of this property by only storing the differences from previous reference frames rather than storing the entire frame. This is implemented by doing motion estimation and compensation.

Most of the fast motion estimation schemes are based on matching algorithms, which are composed of one or more of these basic strategies.

Distance criterion: Distortion criterion for measuring distance between previous block and search area block.Various Criterions are:

- CCF(Cross-Correlation Function)
- MSE(Mean Square Error Function)
- MAE(Mean Absolute Error)
- SAD(Sum of Absolute Difference)
- PDC(Pixel Difference Classification)

MAE(or MAD,SAD are commonly employed due to their simplicity in hardware implementation).

SAD algorithm is used in the proposed architecture.

2.Block Diagram Description

2.1.Schematic block diagram:

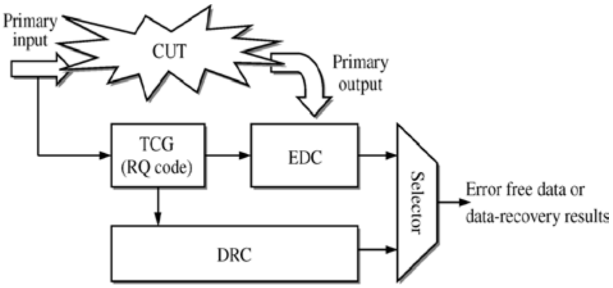

Fig.1:Illustration of circuit

The circuit under test (CUT) consists of inernally connected Processing elements whose inputs are current and reference pixel values of the macro block in a frame.Each Macro block contains four 8X8 luminance blocks and two 8X8 chrominance blocks.The luminance blocks will define the brightness and chrominance blocks define color.

Test Code Generator(TCG) block will generate test vectors from input values based on Residue and Quotient code.The RQ code is used as Built-in-self-Test (BIST) technique.

In place of Circuit Under Test Processing Element is used.The output of CUT as well as TCG are applied to EDC(Error Detection Circuit).EDC will compare outputs of TCG and CUT,if they are same then the output will be'0' which denotes no error.If EDC output is '1' then it indicates an error.If error occurs the data will be recovered from Data Recovery Circuit(DRC).

The selector output may be either from CUT or DRC.

3. Internal architecture:The internal architecture of proposed project is shown below.

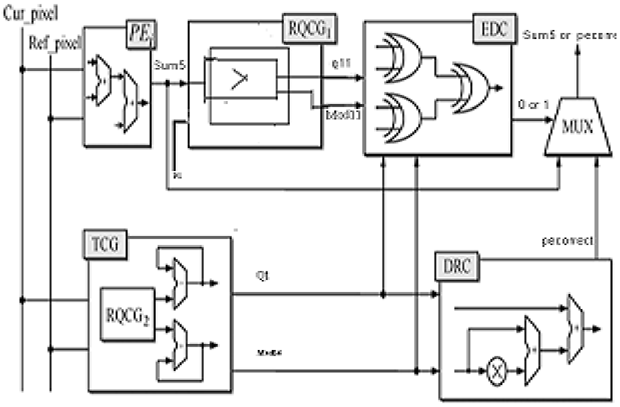

Fig2:Internal architecture based on Bit-Split-Level implem entation.

3.1.PROCESSING-ELEMENT-BLOCK:The circuit in Processing Element(PE) will calculate the Sum of absolute difference(SAD) which is one of the distance criterion used in motion estimation and compensation technique.SAD value is calculated from the formula given below,where Xij and Yij are current and reference pixel values.SAD=Sum5

$$\mathrm{SAD}=\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|X_{ij}-Y_{ij}|$$

3.2.Bit-Split-level implementation code: The residue and quotient values are calculated using this code as follows.Let a and b be the pixel values and q,r be the quotient and residue values.

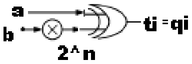

Fig3:To calculate quotient through bit-split-level implementation method.

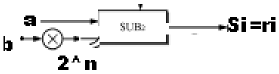

Fig4:To calculate residue using bit-split-level implementation method.

3.3.TEST CODE GENERATOR BLOCK:

The internal architecture of TCG block is shown below.In RQCG block bit split level implementation is carried out. Here Qt=Qt only and Rt=mod14 only.

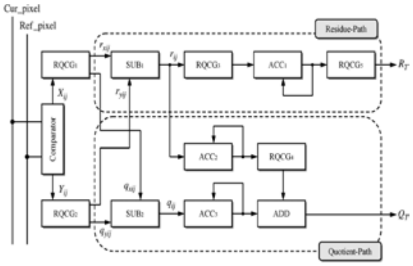

Fig 5:TCG internal circuit to prodce test vectors

As per the figure,first input pixel values are compared using comparator circuit.If there is a difference between current and reference pixels then the proposed code will be applied individually on current and reference pixels and the difference of corresponding residue and quotient values are obtained individually.These values are compared again with RQCG1 block.This procedure is repeated five times by obtaining the differene between the intermediate results which are stored in accumulator register.

3.4.ERROR DETECTION CIRCUIT:

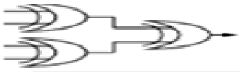

Fig 6:Error Detection circuit with three EX-OR gates

The above EX-OR gate will take inputs from the output of RQCG1 and the below EX-OR gate will have inputs from the output of Test Code Generator circuit.If both RQCG1 and TCG outputs are same then EDC output will be '0',which defines the processing element is error free.If it is '1' then PE has an error and the results will be recovered using Data Recovery Circuit.

3.5.DATA RECOVERY CIRCUIT:This circuit will take input from TCG.The TCG outputs are qt and mod14.DRC circuit will recover the difference between the pixel values using the formula as below.

Pecorrect=qt*p1+mod14

Pecorrect is the output of DRC,qt & mod14 are the outputs of TCG.Where p1=2^k-1;k is an integer.

3.6.MULTIPLEXER

The multiplexer output may be either from PE or DRC depending on EDC output which act as select line.

4.RESULTS AND DISCUSSION:

The outputs of PE,TCG and overall results are shown below.These are obtained by using Xilinx ISE simulator and the program code is written in VHDL.

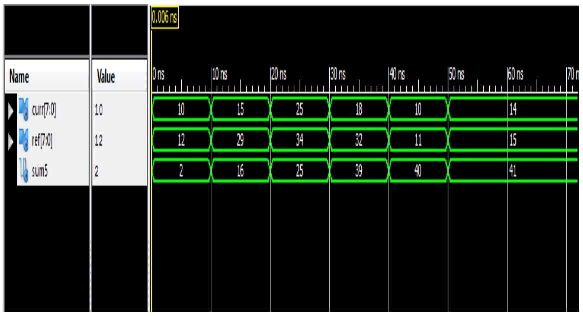

Fig.7:Simulation waveform for Processing element

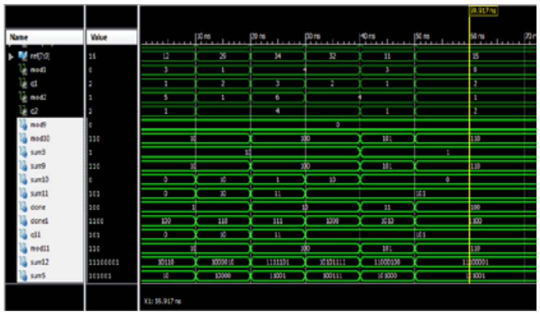

Fig.8:Simulation waveform for Test Code Generator and RQCG1.

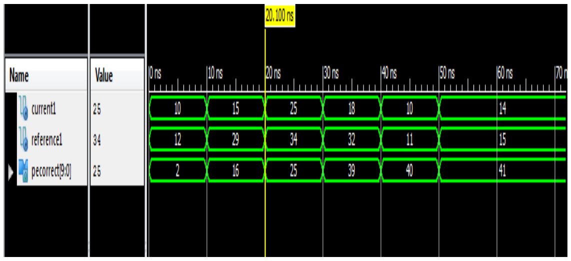

Fig.9:Simulation waveform for selector output.

The following table shows the reduced gate count and improved speed values which are as a result of the use of Bit-split-level implementation code in place of Residue and quotient code.

Table 1: Comparision of specifications

Paramete r	***Gate count***	*Speed(nsec)*
Existing	77300	1986.32
Proposed	12373	550

5.Conclusion:

This project presents BISDSR design for detecting the errors and recovering the data of PEs when Motion Estimation and Compensation technique is used while video compression. Based on the Bit-split-level implementation code, a RQCG-based TCG design is developed to generate the corresponding test codes to detect errors and recover data.The proposed EDDR architecture is implemented by using VHDL. Experimental results indicate that that the proposed architecture can effectivelydetect errors and recover data.Gate Count i.e., circuit complexity is reduced,operation speed is improved.

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